REMARKS

The Office Action of November 30, 2001 was received and carefully reviewed. As a result, reconsideration and withdrawal of the currently pending rejections is requested for the reasons advanced in detail below.

Claims 1-46 were pending prior to the instant amendment. By the above amendments, claims 3, 6 , 8, 12, 13, 14, 18, 19, 24 and 26 have been amended, claims 15, 16 and 28 have been canceled, and new claims 47-54 have been added, according to the requirements of 37 C.F.R.1.173(b); consequently, original claims 1-14, 16-27 and 29 and new claims 30-54 remain pending in the instant application. New claims 47-54 find support in the original specification at column 3, lines 46-63, and column 4, lines 14-37.

With regard to the Examiner's rejection of claims 4 and 6-46, under 35 U.S.C. 112 (first paragraph), as failing to describe in the specification the subject matter of the claims to a sufficient degree to establish to one of skill in the art the inventor had possession of the claimed invention, and with regard to the rejection of claims 1-11 and 18-29, under 35 U.S.C. 103(a), as being obvious in view of the combination of teachings of Parks ('225) and Johary et al ('839), each of these rejections is respectfully traversed for the reasons set forth below.

Specifically, with regard to the rejection of claims 4 and 6-46, under 35 U.S.C. 112 (first paragraph), the Examiner set forth several areas of defects which shall be discussed in the sequence presented in the Office Action of November 30, 2001.

Initially, it is asserted that the phrases "alternating voltage" in claims 34 and 36 and "an AC voltage having an amplitude equivalent to that ... opposite electrode" in patent claims 7 and 23 find no support in the patent specification. However, a review of the voltage depicted in Figures 10A-10C and discussed at column 4, lines 37-52 illustrates just these features. That is, with respect to claims 7 and 23, it is taught that a voltage having the same amplitude as output of the digital memory circuit and a desired frequency such as a vertical synchronizing frequency is applied to an opposite electrode, such that the voltage applied to the liquid crystal is approximately zero on a time average basis. This means, to one of ordinary skill in the art, that the voltage applied to the opposite electrode is an AC voltage. Also, with respect to claims 34 and 36, it is taught that the voltage having the same amplitude as output of the digital memory circuit and a desired frequency such as a vertical synchronizing frequency can be used as the

power source voltage of the digital memory circuit. This also means, to one of ordinary skill in the art, that the power source voltage of the memory circuit is an AC voltage. However, if the Examiner has some other claim language in mind which expresses this feature of the invention in an equivalent way, the Applicant would be willing to discuss such claim language.

The Examiner also states that the phrase "each inverter comprising one p-channel type...and one n-channel thin film transistor" in claims 30, 32, 34, 36, 37 and 39 is also not supported by the patent specification since column 4, lines 62+, states "it is possible that a polarity of a TFT in a pixel matrix portion is only one type that is, a P-channel...or an N-channel type." However, a review of that portion of the patent specification indicates that the section of the patent specification relied upon by the Examiner is directed to the embodiment of Figure 9 which teaches an inverter comprising a pair of resistors and TFT's. In the context of that embodiment, the TFT can be of one conductivity type; however, the patent specification is not limited to that single embodiment. To the contrary, the first embodiment of the invention is illustrated by Figure 8 and is discussed in the patent specification at column 4, lines 8-26. This embodiment clearly illustrates a conventional inverter comprising two TFT's, one P-TFT and an N-TFT (by the direction of the arrows in each TFT of Figure 8).

For the Examiner's convenience, the reference book "Silicon Processing for VSLI ERA", vol 2, pages 368-369, is provided which shows the conventional, well known structure of VLSI inverters as containing both an n- and a p-type TFT. Since 35 U.S.C. 112 (first paragraph) does not require that an applicant set forth that which is conventional, well known and inherent about the invention, see MPEP Chapter 2163(I)(B) and 2163(II)(A)(3)(b) (page 2100-165), the discussion of the conventional inverters in Figure 8 as including two TFTs is deemed sufficient to show one of ordinary skill in the art that the inventor had possession of the subject matter of the claims 30, 32, 34, 36, 37 and 39 at the time of the invention.

In response to the Examiner's discussion regarding the phrases "at least two signal lines electrically connected...pixel electrode" and "wherein different voltages are applied to said...corresponding memory circuit" in claims, 6, 12, 18 and 24, the Applicant has amended the claims to properly refer to the "two signal lines" as "two voltage source lines" which are electrically connected to the memory circuit and not the pixel electrode, as discussed in the patent specification at column 4, lines 14-37, and illustrated in Figure 8.

In response to the Examiner's discussion regarding the phrase "one of source or drain of

the second thin film transistor...said electro-optical modulating layer", the Applicant has amended claim 12 to remove ", and said electro-optical modulating layer."

Finally, with regard to the Examiner's rejection of claim 4 as containing new matter in the recitation of the "digital gradation display device" along with the "time gradation display device" of claim 1, Applicant points out that the patent specification, at column 3, lines 48-68, and the Abstract, as well as Figures 1 and 7, clearly sets forth a time gradation display of an LCD in which digital gradation signals, time-modulated as a start pulse signal, are supplied from the start pulse input signal input terminal "102."

In light of the above arguments and amendments in response to the rejection of claims 4, and 6-46, under 35 U.S.C. 112 (first paragraph), it is respectfully requested that said rejection be withdrawn.

With regard to the rejection of claims 1-11 and 18-26, under 35 USC 103(a), as being obvious in view of the combination of Parks ('225) and Johary et al ('839), the Examiner is contending that Parks discloses a liquid crystal display device comprising first and second substrates, at least one memory circuit connected to a thin film transistor and a pixel electrode, wherein the memory circuit has a first and a second inverter which include a first and second thin film transistor. Parks does not disclose the "time degradation device".

It should be noted, however, that as a result of the above amendments, claims 1-5, 12-14, 16, 17, 24-27, 29, 48 and 50 contain the "time gradation display device" feature; while the remaining claims 6-11, 18-23, 30-47, 49 and 51 set forth the memory circuit configuration including two inverters each having two TFT's (i.e., the embodiment of instant Figure 8) wherein the TFT's are N-channel and P-channel. This embodiment is more advantageous than the Fig. 9 embodiment (or Parks) for reducing power consumption. That is, the power consumption in the case of Figure 8 is much lower than that in the case of Figure 9, due to differences in the circuit configuration.

Specifically, it is pointed out that the combination of Parks ('225) and Johary et al ('839) does not teach or suggest the memory circuit configuration of two inverters each have two TFT's (one N-type and one P-type TFT), i.e., only the inverter structure comprising one TFT and a resistor is taught or suggested by Parks ('225) or Johary ('839). Therefore, the Examiner's rejection of claims 6-11 and 18-23 as being obvious in view of the combination of teachings of Parks ('225) and Johary et al ('839) is inappropriate since each and every feature of the claimed

invention is not taught or suggested by the prior art or by the Examiner, as is required to establish a *prima facie* case of obviousness, see MPEP Chapters 2143 and 2143.01.

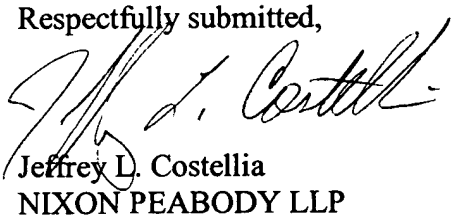
Additionally, with regard to claims 1-5, 12-14, 16, 17, 24-27, 29, 48 and 50, the Johary et al ('839) reference which appears to teach (column 1, lines 23-47; Figures 1A-D) that time gradation display techniques can be used in a display device, also teaches (column 1, lines 48-57; column 3, lines 53-68; column 4, lines 1-20) these display devices do not have the same structure as that of the present invention or Parks. Therefore, one of ordinary skill in the art is provided with no suggestion or motivation to combine the features of Johary et al ('839) with the LCD devices of Parks ('225). Additionally, the Examiner's statement that "it would have been obvious to one of ordinary skill in the art to use Johary's generation means in the Parks' invention so that gradation images can be generated in the Park's display device" does not remedy the failure of either Johary et al ('839) or Parks to reach the presently claimed invention, since such a statement points to no suggestion or motivation in the references themselves to utilize a time gradation display technique in the display device of Parks. As a consequence and for these reasons set forth above, the rejection of claims 1-11 and 18-26, under 35 USC 103(a), as being obvious in view of the combination of Parks ('225) and Johary et al ('839) is believed to be improper and should be withdrawn.

For the reasons set forth above, claims 1-14, 16-27, 29-51 are believed to be in condition for allowance. However, applicant's representative would like to have an interview with the Examiner at the earliest convenience in order to discuss the above amendments and any other issue that in the Examiner's opinion may remain unresolved. The Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby be expedited.

Lastly, it is noted that a separate Petition for Extension of Time (two months) accompanies this response along with a check in payment of the requisite extension of time fee. However, should that petition become separated from this Amendment, then this Amendment should be construed as containing such a petition.

Likewise, any overage or shortage in the required payment should be applied to Deposit Account No. 19-2380 (740756-2204).

Respectfully submitted,



Jeffrey L. Costellia
NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110
(703) 883-0370 (FAX)

JLC/JWM